Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (currently amended): An SRAM device, comprising:

an SRAM array coupled to row peripheral circuitry by a word line and coupled to column peripheral circuitry by bit lines; and

an array low voltage control circuitry that provides an enhanced low operating voltage V_{ESS} to said SRAM array during at least a portion of an active mode thereof wherein said array low voltage control circuitry provides said enhanced low operating voltage V_{ESS} at a higher value than a low operating voltage V_{SS}.

Claim 2 (original): The SRAM device as recited in Claim 1 wherein said array low voltage control circuitry provides said enhanced low operating voltage V_{ESS} only during a WRITE operation.

Claim 3 (original): The SRAM device as recited in Claim 1 wherein said array low voltage control circuitry provides said enhanced low operating voltage V_{ESS} during all of said active mode.

Claim 4 (original): The SRAM device as recited in Claim 1 wherein said array low voltage control circuitry provides said enhanced low operating voltage V_{ESS} during all modes.

Claim 5 (original): The SRAM device as recited in Claim 1 wherein said array low voltage control circuitry provides said enhanced low operating voltage V_{ESS} based on a factor selected from the group consisting of:

a process corner,

a transistor parameter,

a mode of operation, and

a value of a high supply voltage.

Claim 6 (original): The SRAM device as recited in Claim 1 wherein said array low voltage control circuitry provides said enhanced low operating voltage V_{ESS} at a higher value when based on a strong n process corner.

Claim 7 (original): The SRAM device as recited in Claim 1 wherein said array low voltage control circuitry provides said enhanced low operating voltagè V_{ESS} at a lower value during a READ operation than during a WRITE operation.

Claim 8 (original): The SRAM device as recited in Claim 7 wherein said array low voltage control circuitry only provides said lower value for an addressed column of said SRAM array.

Claim 9 (original): The SRAM device as recited in Claim 1 wherein said array low voltage control circuitry employs an active component to provide said enhanced low operating voltage V_{ESS}.

Claim 10 (original): The SRAM device as recited in Claim 1 wherein said array low voltage control circuitry provides said enhanced low operating voltage V_{ESS} employing a component selected from the group consisting of:

a diode,

a transistor,

a fuse,

a ROM,

a voltage regulator, and

logic circuitry.

Claim 11 (canceled):

Claim 12 (currently amended): A method of operating an SRAM device, comprising:

employing in an integrated circuit an SRAM array coupled to row peripheral circuitry by a word line and coupled to column peripheral circuitry by bit lines; and

providing an enhanced low operating voltage V_{ESS} to said SRAM array during at least a portion of an active mode wherein said array low voltage control circuitry provides said enhanced low operating voltage V_{ESS} at a higher value than a low operating voltage V_{SS}.

Claim 13 (original): The method as recited in Claim 12 wherein said providing only occurs during a WRITE operation.

Claim 14 (original): The method as recited in Claim 12 wherein said providing occurs during all of said active mode.

Claim 15 (original): The method as recited in Claim 12 wherein said providing occurs during all modes.

Claim 16 (original): The method as recited in Claim 12 wherein said providing is based on a factor selected from the group consisting of:

a process corner,

a transistor parameter,

a mode of operation, and

a value of a high supply voltage.

a process corner,
a transistor parameter,
a mode of operation, and
a value of a high supply voltage.

Claim 17 (original): The method as recited in Claim 12 wherein said enhanced low operating voltage V_{ESS} is provided at a higher value based on a strong n process corner.

Claim 18 (original): The method as recited in Claim 12 wherein said enhanced low operating voltage V_{ESS} is provided at a lower value during a READ operation than during a WRITE operation.

Claim 19 (original): The method as recited in Claim 18 wherein said lower value is only provided for an addressed column of said SRAM array.

Claim 20 (original): The method as recited in Claim 12 wherein said providing includes employing an active component to provide said enhanced low operating voltage V_{ESS}.

Claim 21 (original): The method as recited in Claim 12 wherein said providing includes employing a component selected from the group consisting of:
a diode,
a transistor,
a fuse,
a ROM,
a voltage regulator, and
logic circuitry.